**ABSTRACT**

A Solenoid-type Inductors have been realized using electroplating technique mainly used for 2Ghz band CMOS RF VCO applications. The integrated spiral inductor has low Q factor due to substrate loss and skin effects. And It also occupies large area compared to solenoid-type inductor. The direction of flux of the solenoid-type inductor is parallel to the substrate, which can lower substrate loss and other interference with integrated passive components. In this research, Solenoid-type inductors are simulated and modeled as equivalent circuit for CMOS RF VCO based on extracted S-parameters. The electroplated solenoid-type inductors are fabricated on both a standard silicon substrate and glass substrate by thick PR photolithography and copper electroplating. The achieved inductance varies range from 1nH to 5nH, and maximum Q factor over 10. The inductors are scheduled to be integrated on CMOS RF VCO with RF MEMS capacitor for future.

Keywords: Electroplating, solenoid, inductors, VCO, RF, MEMS, capacitor

1. INTRODUCTION

As the mobile communication market is ever-growing, PLL frequency synthesizer get tight specification for phase noise to lower channel interference. Low phase noise VCO consists of passive LC tank and negative gm active circuit. Many researches have focused on good quality integrated passive components. Most of integrated inductors are spiral-types [1]. For Silicon-based CMOS RF IC’s, the inductor quality factor (Q) degrades at high frequency due to both skin and substrate effect. There are some approaches about substrate issues, such as use of high–resistivity substrate(150-200 $\Omega \cdot \text{cm}$)[2], and etching a pit in the silicon substrate under the inductors[3]. These methods add extra processing cost and are not compatible with standard CMOS process. For skin effect, which means high frequency current, flows on metal surface, thick gold metallization [1], multiple metal layers in parallel [4], or copper metallization [5] have been reported. Even though these methods are compatible with standard CMOS process, the inductor quality factor is still lower than 10. While on-chip bondwire inductor [6] shows superior performance compared to spiral inductor, Repeatability and Robustness avoid its application on RF passive components.

Recently, Solenoid-type inductors have been reported for wireless communication applications [7]. Superior high Q inductor is obtained from high conductive copper material and high aspect-ratio thick photoresist.

In this work, we had fabricated solenoid inductors occupying small area by copper electroplating and photolithography. Based on the extracted lumped equivalent circuit of inductor, the simulation was done for 2Ghz band CMOS VCO. The capacitor in LC tank was implemented by MOS capacitor instead of p+/n junction capacitor. The CMOS active circuit of VCO with MOS capacitor is under fabrication supported by DEC MPW Project. Later, This MOS capacitor will be replaced by MEMS capacitor [8] using flip-chip bonding technique.

2. SOLENOID-TYPE INDUCTOR DESIGN

For a solenoid-type inductor, the inductance L can be represented with a simple equation, neglecting substrate and fringing effect.

$$L = \frac{4\pi \times 10^{7} \times n^{2} \times A}{n \times p}$$

Where $n$ is the number of coil turn, $A$ is the cross-sectional area and $p$ is pitch between turns.
This analytical equation of solenoid inductor is not adequate for high frequency application because high frequency current flows on conductor surface by skin effect. In order to better understand all electromagnetic effects on inductor, simulation is necessary because the problem is too complex to be solved analytically. The only way to fully simulate all the effects is a full three-dimensional (3-D) finite-element simulation. This FEM simulation, however, is time-consuming. Simulation was done to get insight into which structure dimension parameters are dependent on inductance.

Solenoid inductor has rectangular cross-sectional shape. The simulated structure is the same as the fabricated one. Ground-signal-Ground probe pattern is also included in simulation. Copper plated structure is constructed on glass wafer. The simulations were done with \(a=b=20\mu m\), \(w=80\mu m\), \(h=10\mu m\) and \(n=10, 20, 30\) and \(40\) respectively with commercially available software, HFSS [9]. It takes several hours and large amount of virtual memory to simulate all frequency in 10GHz. So we choose six frequency points. It was enough to see the inductance and quality factor. As seen from fig 3, the inductance value is linearly dependent on the number of turn. But as frequency increases, the inductance is no more dependent on it proportionally. Simulation result shows the quality factor is over 10, and the inductance is range from 0.7nH to 2.3nH.
3. FABRICATION

Fig 4. Fabrication Steps: (a) Ti 200Å /Au 2000Å seed deposition, (b) Photolithography for electroplating base mold using first mask, (c) copper plating, (d) post(via) pattern photolithography using second mask, (e) temperature curing and seed layer evaporation (2000Å Au), (f) Air bridge pattern photolithography using third mask, (g) Air bridge copper plating, (h) PR and seed layer removal.

Fig 4 shows solenoid inductor fabrication steps. Pyrex 7740 glass wafer was used as substrate, onto which a seed layer of Ti(200Å) /Au (2000Å) was deposited using thermal evaporator. AZ4620 positive photo resists were used to produce 5µm thick base and air bridge, 10µm thick post (via) electroplating mold. After base mold photolithography, 5µm thick base copper was electroplated from the gold seed layer. The electroplating was achieved by commercially available plater machine, CW-3. This machine was modified from bump plater controlled by software. Given plating area and current density, the target plating thickness could be achieved by software timing control. After post (via) plating, two consequent photo resist layers were cured at oven to dehydrate. Then a gold seed layer was deposited for Air Bridge. In MESD method [10], air bridge was formed by overplating without additional air bridge photomask.

Following air bridge plating, photoresist was stripped with acetone, and the seed layer was removed by commercial gold etchant. The photo resist residue on seed layer was also removed by O2 Plasma. In this same method, base and post (via) mold were removed. Exposure system was Kalsuss MA6 aligner by which 5µm thick and 10µm thick photo resist were exposed at 168mj/µm2, 360mj/µm2 respectively.

Fig 5. SEM photograph of 9 turns, copper plated solenoid inductor.
4. MEASUREMENT

The inductors were measured using HP8510B network analyzer and cascode mircotech RF probe. The 2 ports S-parameter measurements were performed from 500Mhz to 10Ghz. Open pad was also measured in order to de-embed pad capacitance and resistance from inductor.

Fig 6. (a) Inductance for various dimension, (b) measured Q factors, (c) inductance and Q factor for \(a=b=30\mu m, w=80\mu m,\) with 30 turns. (d) inductance ratio for two different number of turns.(L39 and L40)
As shown fig 6 (a), inductance value is linearly increased by number of turns such as L39 and L40, L41 and L38. Fig 6 (d) shows the detailed plot about inductance. It shows the inductance increasing factor is 1.85 as number of turns of inductor increases twice. Figure 6 (c) shows inductor with $a=b=30\mu m, w=80$ and $n=30$, has inductance $1.95nH$ and Q factor as 9.7 at 2.4Ghz. Inductor has self-resonance frequency over 7Ghz.

![Inductance Comparison](image1.png)

![Q factor comparison](image2.png)

Fig 7. (a) Inductance comparison between simulated and measured. (b) Q factor comparison between two.

In Fig.7 the measured inductance is about 20% higher than the simulated result. This was partly due to the fabrication variation such as post (via) height or bridge width. For lower quality factor, the CuO was blamed to increase contact resistance when G-S-G RF probe was probing on the pad.

To apply solenoid-type inductor for CMOS RF VCO, a small-signal equivalent circuit in Fig.8 has been used. The electrical parameters were extracted by Ansoft Serenade’s linear optimizer with the equivalent circuit, where skin depth effect of resistance is also considered.[10]. The equivalent circuit parameters are summarized in Table I.

![Equivalent Circuit](image3.png)

Fig 8. Equivalent circuit of the solenoid inductor on a glass substrate.
Table I. Equivalent circuit parameters.

<table>
<thead>
<tr>
<th>Device</th>
<th>L (nH)</th>
<th>a</th>
<th>b</th>
<th>C f (fF)</th>
<th>C p1 (fF)</th>
<th>C p2 (fF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>L37</td>
<td>1.794</td>
<td>3.712</td>
<td>0.140</td>
<td>4.019</td>
<td>0.012</td>
<td>0.035</td>
</tr>
<tr>
<td>L38</td>
<td>2.381</td>
<td>2.923</td>
<td>3.410</td>
<td>0.437</td>
<td>0.024</td>
<td>0.024</td>
</tr>
<tr>
<td>L39</td>
<td>1.375</td>
<td>3.071</td>
<td>1.600</td>
<td>0.437</td>
<td>0.024</td>
<td>0.024</td>
</tr>
<tr>
<td>L40</td>
<td>2.679</td>
<td>2.366</td>
<td>4.936</td>
<td>0.437</td>
<td>0.024</td>
<td>0.024</td>
</tr>
<tr>
<td>L41</td>
<td>1.238</td>
<td>1.856</td>
<td>0.744</td>
<td>0.437</td>
<td>0.024</td>
<td>0.024</td>
</tr>
<tr>
<td>L42</td>
<td>0.499</td>
<td>0.199</td>
<td>1.489</td>
<td>0.437</td>
<td>0.024</td>
<td>0.024</td>
</tr>
</tbody>
</table>

5. VCO DESIGN

Based on the equivalent circuit of solenoid-type inductor, RF CMOS VCO was designed and simulated. The oscillator circuit schematic is shown in Fig 9 (a). Solenoid type inductor is parallel with PMOS capacitor (P3,P4) . Two NMOS transistors, N1 and N2 are coupled in positive feedback to provide a negative resistance. With inductance value of 2.4nH, the total capacitance must be 1.8pF to obtain an oscillation frequency of 2.4Ghz. The 2-pF tunable capacitor is made as PMOS transistor (P3,P4) tied source and drain together. It is known that PMOS capacitor low parasitic resistance compared to p+/n-/n+ junction capacitor.[12] For needed capacitance 1pF, PMOS transistor area is 160 μ. Simple calculation shows that PMOS capacitor have \( W=160\text{μm}/L=0.5\text{μm} \) for 0.25μm digital CMOS process with gate oxide thickness,55Å.
6. CONCLUSION

A solenoid-type inductors were simulated and realized by electroplating and photolithography. Conventional analytical equation of inductance was not adequate for solenoid-type inductor mainly used in high frequency application. So we choose the commercial available FEM software, HFSS which could help get the exact analysis of three-dimensional structure. Based on the extracted S parameter from HFSS simulation, we had simulated RF CMOS VCO circuit. The fabricated solenoid inductance value was range from 0.7nH to 2.8nH. The occupied area was 120um x 780um for 1.5nH. Through post-CMOS process, solenoid-type inductor will be integrated through pad opening. Now that solenoid type inductor have high Q factor over spiral inductor, solenoid inductor integrated VCO has very low phase noise and meet the strict requirement in communication transceiver. As copper metallization have been focused on the next candidate in ULSI technology, the fabrication process for copper plated solenoid inductor would be adapted as standard CMOS process for future.

7. ACKNOWLEDMENTS

The authors would like to thank to all staffs of ISRC and Mtec. This work was supported by KETI(Korea Electronics Technology Institute) G7 project under Ministry of commerce, Industry and energy on grant ISRC 2000-X-6119. And this work was also partly funded from BK21(Brain Korea 21) by Ministry of education.

8. REFERENCES

8. Seonho seok, Chul Nam, Kukjin Chun,” A MEMS variable capacitor for one-chip RF frond end”, SPIE ISMA2000, to be published.


NAM
4230-1
8
Chul Nam(4230-1), Seonho Seok(4203-3)
Seoul National Univ. San56-1, Shinlim-Dong, Kwannak-Gu,
Seoul 151-741, Korea (Manuscripts included)

SPIE Proceedings
P.O.Box 10, Bellingham, WA98227-0010 USA